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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,340	02/25/2004	Hiroyuki Akatsu	FIS920030411US1	2339

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INTERNATIONAL BUSINESS MACHINES CORPORATION
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BLDG. 300-482
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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/708,340	AKATSU ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,10 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,10 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 04/08/2007 claims 8, 10, and 21-23 are active in this application.

Claim(s) 1-7, 9, and 11-20 have been cancelled.

Remarks

2. Applicant's argument(s), filed 04/08/2007, have been fully considered, but are not persuasive. See the following rejection for detail.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim(s) 8, and 10 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 5,481,120 to Mochizuki et al.

Regarding claim 8, Mochizuki discloses a bipolar transistor, shown in fig. 67, comprising:

a collector 3 including a frustum-shaped collector pedestal having an at least substantially planar upper surface, a lower surface, and a slanted sidewall extending between said upper surface and said lower surface, wherein said upper surface has an area substantially less than an area of said lower surface;

an intrinsic base 5 overlying all of said area of said upper surface of said collector pedestal 3;

an emitter 8 overlying said intrinsic base 5;

an extrinsic base 6 conductively connected to said intrinsic base 5; and

a first dielectric region 4' (figs. 67a-c) laterally adjacent to said emitter 8; and

a second dielectric region 21 laterally adjacent to said collector pedestal 3, an opening (in which the collector 3, the base 5 and the emitter 8/9 are formed) extending through said first and second dielectric regions 4' and 21, respectively, said opening having a wall extending through said first and second dielectric regions, said emitter 8 having an edge referenced to said wall of said opening and said collector pedestal 3 having an edge referenced to said wall, such that said emitter 8 is aligned with said collector pedestal 3.

Regarding claim 10, Mochizuki discloses the bipolar transistor wherein said intrinsic base 5 includes a layer of a single-crystal semiconductor which forms a

heterojunction with at least one of said emitter and said collector pedestal. See fig. 67.

Claim Rejections - 35 U.S.C. § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim(s) 21 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Mochizuki et al. (US 5,481,120), in view of Park (US 6,287,930).

Regarding claim 21, Mochizuki discloses a bipolar transistor comprising all claimed limitations, including a conductive collector contact 12, said collector further including a first active area 2, 3 and a second active area 2 disposed in a single-crystal semiconductor region, each of said first and second active areas having major surfaces extending in lateral directions defining a major surface of said semiconductor region, said first active area underlying said collector pedestal 3 and said second active area being separated in at least one of said lateral directions from said first active area, wherein said collector contact via 12 overlies said second active area. See figs. 1, 2, 5-8, 27, 50, 65.

Mochizuki fails to teach a dielectric-filled shallow trench isolation wherein said first active area 2 underlying said collector pedestal 3 and said second active area 2

being separated in at least one of said lateral directions from said first active area 2 by said shallow trench isolation.

Park discloses a bipolar transistor shown in figs. 3-13, comprising a shallow trench isolation 77 or 16 (figs. 3, 13) filled with dielectric layer 77/16 and a conductive collector contact via 97, wherein a first active area underlying a collector pedestal 13 (between trenches 75, figs. 7-8) and said second active area being separated in at least one of said lateral directions from said first active area by said shallow trench isolation 77/16, and wherein said collector contact via 97 overlies said second active area. See figs. 3, 13.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Mochizuki so that it would further include a dielectric-filled isolation trench as that/those of Park in order to provide electrical isolation to the device, and to obtain a more highly integrated bipolar junction transistors having improved electrically characteristics. See col. 2, lines 13-27, and lines 54-58 of Park.

7. Claim(s) 22 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Mochizuki et al. (US 5,481,120).

Regarding claim 22, Mochizuki discloses the bipolar transistor shown in fig. 67 comprising all claimed limitations as discussed in the base claim above, including extrinsic base 6. The extrinsic base 6 in fig. 67 does not show a raised portion.

However, figs. 27 show(s) extrinsic base structure 6/16 (fig. 27) including raised extrinsic base, wherein a wall of said raised portion of said extrinsic base 6/16 is aligned with said wall of said opening in said first and second dielectric regions.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention illustrated by fig. 67 so that the extrinsic base 6 would further include raised portion(s), as that/those shown in figs. 27, in order to increase the carrier concentration and the mobility in the extrinsic base region, which make it possible to fabricate a very high speed bipolar transistor being small in the base resistance and in the base-collector capacitance (see col. 17, lines 38-44).

wherein at least a portion of said extrinsic base 6 is raised above an upper surface of said intrinsic base 5, wherein a wall of said raised portion of said extrinsic base 6 is aligned with said wall of said opening in said first and second dielectric regions 26/21.

8. Claim(s) 21 and 23 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Mochizuki et al. (US 5,481,120), in view of Harame et al. (US 5,101,256).

Regarding claim 21, Mochizuki discloses a bipolar transistor comprising all claimed limitations, including a conductive collector contact 12, said collector further including a first active area 2, 3 and a second active area 2 disposed in a single-crystal semiconductor region, each of said first and second active areas having major surfaces extending in lateral directions defining a major surface of said semiconductor region, said first active area underlying said collector pedestal 3 and said second active area being separated in at least one of said lateral directions from said first active area, wherein said collector contact via 12 overlies said second active area. See figs. 1, 2, 5-8, 27, 50, 65.

Mochizuki does not explicitly discuss a dielectric-filled shallow trench isolation wherein said first active area 2 underlying said collector pedestal 3 and said second active area 2 being separated in at least one of said lateral directions from said first active area 2 by said shallow trench isolation.

Harame discloses a bipolar transistor shown in figs. 1A-C, comprising a shallow trench isolation 18B/C filled with dielectric layer (SiO_2, col. 5, lines 32-38) and a conductive collector contact via 16, wherein a first active area underlying a collector pedestal 14 and a second active area (portion of layer 12 underneath the collector contact via 16) being separated in at least one of said lateral directions from said first

active area by said shallow trench isolation 18B/C, and wherein said collector contact via 16 overlies said second active area.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Mochizuki so that it would further include a dielectric-filled isolation trench as that/those of Harame in order to provide electrical isolation to the device, and to obtain a more highly integrated bipolar junction transistors having improved electrically characteristics, hence to increase the performance of the device.

Regarding claim 23, Mochizuki discloses the bipolar transistor comprising all claimed limitations, as discussed above, except for further comprising a solid dielectric spacer spacing said raised portion of said extrinsic base from said emitter, said solid dielectric spacer including (a) a first dielectric spacer wholly contacting a wall of said raised portion of said extrinsic base, and (b) a second dielectric spacer contacting an inner wall of said first dielectric spacer remote from said raised portion of said extrinsic base.

Harame discloses a bipolar transistor, shown in figs. 1A-C, comprising a solid dielectric spacer 34&36 spacing a raised portion 32B&24 of an extrinsic base 32B&24 from an emitter 40, said solid dielectric spacer 34&36 including (a) a first dielectric spacer 34 wholly contacting a wall of said raised portion 32B of said extrinsic base

32B&24, and (b) a second dielectric spacer 36 contacting an inner wall of said first dielectric spacer 34 remote from said raised portion of said extrinsic base 32B&24.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Mochizuki so that it would further include a solid dielectric spacer, as that taught by Harame in order to better provide electrical isolation between the emitter and the raised base region, hence to increase the performance of the device. See col. 7, lines 57-64 of Harame.

Conclusion

9. **THIS ACTION IS MADE FINAL.** A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday 9:00am - 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke, can be reached on (571)272-1657. The fax numbers for all communication(s) is (571)273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

Dao H. Nguyen
Art Unit 2818
June 13, 2007

STEVEN LOKE
SUPERVISORY PATENT EXAMINER